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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,232	02/18/2004	Doug Pan	37829.1717	2231
20322	7590	05/28/2004		
SNELL & WILMER ONE ARIZONA CENTER 400 EAST VAN BUREN PHOENIX, AZ 850040001			EXAMINER TRAN, MICHAEL THANH	
			ART UNIT 2818	PAPER NUMBER

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/708,232

Applicant(s)

PAN, DOUG

Examiner

Michael T Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 February 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-59 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 52-54 is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-8, 13-44, 48 and 56-59 is/are rejected.
- 7) ☒ Claim(s) 4, 9-12, 45-47, 49-51 and 55 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 0204
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

1. In response to the Communications dated February 18, 2004, claims 1-59 are active in this application.

Information Disclosure Statement

2. The information disclosure statement filed February 18, 2004 has been considered.

Claim Objections

3. Claims 9-12, 45-47, 49-51, 55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

It appears that the phrases "said predriver circuit", "said pull-up predriver transistor", and "said pull-down predriver transistor", in claim 4, lack antecedent basis.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-3, 6, 13-17, 24-37, 39-42, 44, 48, and 56-59 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, 4, 14-28, 31-33, 41, 42, and 44 of U.S. Patent No. 6,714,462 ['462]. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the reasons set forth below.

6. Claims 1-3, 6, 13-17, 24-37, 39-42, 44, 48, and 56-59 are rejected in view of claims 1, 2, 4, 14-28, 31-33, 41, 42, and 44 of the '462 patent. Similar to the claimed invention, claim 1 of the patent recites "...an output buffer...predriver circuit...output driver circuit...a slew rate control circuit...". Claim 4 of the patent recites "...a first amplifier...a second amplifier..." Claim 14 of the patent recites "...a slew rate control circuit...first amplifier...first current source..." Similar reasons apply to other claims. As can be seen, the patent protection for the claimed invention has already been granted to the earlier filed application.

Claim Rejections – 35 U.S.C. § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-

- (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
- (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

8. Claims 1 and 5 are rejected under 35 U.S.C 102(b) as being anticipated by Keeth [U.S. Patent #5,872,736].

With respect to claim 1, Keeth discloses, **in figure 9**, an output buffer **[200]** configured for use within DRAM applications, said output buffer comprising: an output driver circuit **[either 214 or 216]** configured for providing an output signal for said output buffer; and a slew rate control circuit **[210]** coupled to said output driver circuit and configured for receiving a drive input signal and for controlling a slew rate of said drive input signal based on a level of voltage provided from a power supply **[via source/drain 218]** to said output driver circuit.

With respect to claim 5, Keeth discloses, **in figure 9**, that the output driver circuit comprises: a pull-up transistor **[within 214]** having an input terminal configured for coupling to the power supply **[via source/drain 218]**, and a control terminal coupled to said slew rate control circuit **[via 206]**; and a pull-down transistor **[within 216]** having an

input terminal configured for coupling to a ground connection [via 218], an output terminal coupled to an output terminal of said pull-up transistor [via 208], and a control terminal [via 208] coupled to said slew rate control circuit.

9. Claims 7 and 8 are rejected under 35 U.S.C 102(b) as being anticipated by Keeth [U.S. Patent #5,872,736].

With respect to claim 7, Keeth discloses, in figure 9, an output buffer [200] configured for use in a memory applications, said output buffer comprising: an output driver circuit [either 214 or 216] configured for providing an output signal for said output buffer, wherein said output driver circuit comprises: a pull-up transistor [within 214] having an input terminal [via source/drain of 218] configured for coupling to a power supply; and a pull-down transistor [within 216] having an input terminal [via 218] configured for coupling to a ground connection, an output terminal [via 208] coupled to an output terminal of said pull-up transistor; and a slew rate control circuit [210] coupled to control terminals of said pull-up transistor and said pull-down transistor of said output driver circuit and configured for controlling a slew rate of a drive input signal.

With respect to claim 8, Keeth discloses that the slew rate control circuit is configured for controlling a slew rate of a drive input signal based on a level of voltage in said power supply provided to said output driver circuit [via source/drain of 218].

Allowable Subject Matter

10. Claims 52-54 are allowable over the prior art of record.

11. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- ❖ Output buffer further comprises a predriver circuit comprising: a pull-up predriver circuit for providing a pull-up input signal for controlling said pull-up transistor of said output driver circuit; and pull-down predriver circuit for providing a pull-down input signal for controlling said pull-down transistor of said output driver circuit.
- ❖ Said slew rate control circuit comprises a first amplifier circuit configured for controlling a slew rate of a pull-up input signal and providing said controlled pull-up input signal to said output driver circuit; and a second amplifier circuit configured for controlling a slew rate of a pull-down input signal and providing said controlled pull-down input signal to said output driver circuit.
- ❖ Output buffer further comprises a predriver circuit configured for providing said drive input signal.
- ❖ Wherein said first amplifier circuit comprises a first operational transconductance amplifier, and said second amplifier circuit comprises a second operational transconductance amplifier.
- ❖ Wherein said first amplifier circuit is configured with a first voltage controlled current source, and said second amplifier circuit is configured with a second voltage-controlled current source.
- ❖ Wherein at least one of said first current source and said second current source comprises: a first fixed current source coupled to an output of said first transistor

and said second transistor; and a second fixed current source coupled to said third transistor.

- ❖ Wherein said comparing said level of voltage of the power supply with said reference voltage is conducted within a voltage-controlled current source.
- ❖ Receiving said slew rate control circuit said input drive signal from a predriver circuit; determining a level of voltage of said power supply for the output buffer.
- ❖ Determining said level of voltage of said power supply comprises scaling down voltage of said power supply to provide said level of voltage.
- ❖ Wherein said step of controlling said slew rate comprises adjustment of a slew rate in at least one of a pull-up drive signal and a pull-down drive signal.
- ❖ Wherein said DRAM output buffer further comprises an output driver circuit configured for receiving at least one of said controlled pull-up signal and said controlled pull-down signal and for providing an output signal.
- ❖ A slew rate control circuit configured for receiving at least one input control signal and for controlling a slew rate of a controlled drive signal based on voltage changes in a power supply, said slew rate control circuit comprising a first amplifier circuit for receiving a pull-up input signal, and a second amplifier circuit for receiving a pull-down input signal.

Conclusion

12. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited

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to assist the Examiner in the prosecution of this case.

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

14. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.



Michael T. Tran
Art Unit 2818
May 27, 2004